Amendments to the Drawings

The attached six drawing sheets include changes to FIGs. 1A-B, 2, 3A-C, 4, 5, and 6A-C. For each of these drawings, the designation "Prior Art" has been inserted.

REMARKS/ARGUMENTS

This responds to the Office Action, dated March 10, 2005. Claims 1 - 67 are pending in this application.

Drawings

The Examiner stated that FIGs. 1A-B, 2, 3A-C, 4, 5, and 6A-C should be designated by a legend such as "Prior Art" because only that which is old is illustrated. In response, Applicant has amended these drawings to include this legend. Six replacement sheets are included with this amendment.

Claim Rejections - 35 USC § 103

The Examiner rejected Claims 1-4, 14, 42-44, 46, 47, 49-52, 54, and 58-61 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,150,619 to Reynolds in view of U.S. Patent No. 6,301,649 to Takasugi, and further in view of U.S. Patent No. 6,496,192 to Shreesha, and further in view of U.S. Patent No. 4,189,767 to Ahuja, and in view of what the Examiner considers to be Applicant-admitted prior art.

Regarding claim 1, the Examiner cited Reynolds in view of Takasugi and Shreesha as grounds for his rejection. Claim 1 requires at least two data elements that are consecutive in a first order be stored in parallel to at least two memory devices and at least two data elements that are consecutive in a second order be retrieved in parallel from the at least two memory devices. The Examiner already has stated that Reynolds does not disclose the storage and retrieval of consecutive data units in parallel. As to Takasugi, the Examiner stated that while Takasugi does not disclose the storage of data elements that are consecutive, it does disclose the storage and retrieval of data elements in parallel.

Applicant respectfully disagrees with this interpretation of Takasugi. The cited portions of Takasugi disclose a memory comprised of a plurality of banks that uses bank interleaving. It claims an ability to obtain a high-speed serial access to continuous address bits on different rows to thereby operate write addresses. As a result, the continuous high-speed serial access in the column direction can be performed by the memory. Thus, the cited

portions of Takasugi disclose serial access to image data, but not the parallel storing and retrieving required by claim 1.

Similarly, the cited portions of Shreesha do not disclose this parallel storing and retrieving requirement. In the cited portions of Shreesha, a memory system operates by storing several adjacent pixel elements along one dimension of the image into the memory in a single first memory write operation. While this first write operation is being performed to one bank of the memory device, the next subsequent pixel elements are being prepared to be written into the other bank of the memory device. Thus the parallel storing and retrieving requirement of claim 1 is not present in the cited portions of Shreesha.

Because the cited portions of neither Reynolds, Takasugi nor Shreesha disclose this parallel storing and retrieving requirement of claim 1, this claim is not rendered obvious by their combination.

Moreover, Applicant contends that it was not proper to combine Shreesha with Reynolds or Takasugi. In order to combine references, the Examiner is required to show that there was a teaching, suggestion, or motivation to combine them. The reason given by the Examiner for combining Shreesha is that it allows "blocks of image data to be fetched without latency." (Office Action, page 3). However, Applicant respectfully contends that this is not a valid teaching, suggestion, or motivation. As stated by the Federal Circuit Court of Appeals in Cardiac Pacemakers, Inc., v. St. Jude Medical, Inc., 381 F.3d 1371 (Fed. Cir. 2004):

> "Recognition of a need does not render obvious the achievement that meets that need. There is an important distinction between the general motivation to cure an uncured disease (for example, the disease of multiple forms of heart irregularity), and the motivation to create a particular cure."

In our case, the cited portions of Shreesha generally deal with the filtering or re-sizing of images and acknowledge a need to filter the image data faster. However, the mere recognition of this need by Shreesha does not render obvious Applicant's particular invention in claim 1 for achieving greater speed, *i.e.,* including the storing and retrieving of consecutive data elements in parallel in two different orders. Thus for this additional reason, claim 1 is not obvious under Reynolds in view of Takasugi and Shreesha. Withdrawal of the rejection to claim 1 is requested.

Claims 2 - 46 depend directly or indirectly from claim 1, and include all limitations of claim 1. Having established that claim 1 was not rendered obvious in view of the cited references, dependent claims 2 - 46 similarly are not obvious. Withdrawal of the rejections to claims 2 - 46 also is requested.

Regarding independent claim 47, the Examiner cited Reynolds in view of Takasugi and Shreesha as grounds for his rejection, incorporating the same arguments as those used in rejecting claim 1. In claim 47, there is the requirement that at least two pixels that are horizontally adjacent are stored in parallel, and that at least two pixels that are vertically adjacent are retrieved in parallel. Because the cited portions of neither Reynolds, Takasugi nor Shreesha disclose this parallel storing and retrieving requirement of claim 47, (as discussed more fully above) this claim is not rendered obvious by their combination. Additionally, for the reasons discussed above, it was not proper to combine Shreesha with Reynolds or Takasugi, because there was no showing of a teaching, suggestion, or motivation to combine them. Withdrawal of the rejection to claim 47 is requested.

Claims 48 - 50 depend directly or indirectly from claim 47, and include all limitations of claim 47. Having established that claim 47 was not rendered obvious in view of the cited references, dependent claims 48 - 50 similarly are not obvious. Withdrawal of the rejections to claims 48 - 50 also is requested.

Regarding independent claim 51, the Examiner cited Reynolds in view of Takasugi and Shreesha as grounds for his rejection, incorporating the same arguments as those used in rejecting claim 1. In claim 51, there is the requirement that a buffer store multiple data elements in parallel to respective memory pages and retrieve multiple data elements in parallel from respective memory pages. Because the cited portions of neither Reynolds, Takasugi nor Shreesha disclose this parallel storing and retrieving requirement of claim 51, (as discussed more fully above) this claim is not rendered obvious by their combination. Additionally, for the reasons discussed above, it was not proper to combine Shreesha with Reynolds or Takasugi, because there was no showing of a teaching, suggestion, or motivation to combine them. Withdrawal of the rejection to claim 51 is requested.

Claims 52 - 58 depend directly or indirectly from claim 51, and include all limitations of claim 51. Having established that claim 51 was not rendered obvious in view of the cited

references, dependent claims 52 - 58 similarly are not obvious. Withdrawal of the rejections to claims 52 - 58 also is requested.

Regarding independent claim 59, the Examiner cited Reynolds in view of Takasugi and Shreesha as grounds for his rejection, incorporating the same arguments as those used in rejecting claim 1. In claim 59, there is the requirement that a memory controller store pixel data for multiple pixels in parallel to respective memory pages and retrieve pixel data for multiple pixels in parallel from respective memory pages. Because the cited portions of neither Reynolds, Takasugi nor Shreesha disclose this parallel storing and retrieving requirement of claim 59, (as discussed more fully above) this claim is not rendered obvious by their combination. Additionally, for the reasons discussed above, it was not proper to combine Shreesha with Reynolds or Takasugi, because there was no showing of a teaching, suggestion, or motivation to combine them. Withdrawal of the rejection to claim 59 is requested.

Regarding independent claim 60, the Examiner cited Reynolds in view of Takasugi and Shreesha as grounds for his rejection, incorporating the same arguments as those used in rejecting claim 1. In claim 60, there is the requirement for storing a first pixel and a second pixel in parallel in a first memory and a second memory, respectively, and storing a third pixel and a fourth pixel in parallel in the second memory and the first memory, respectively. Because the cited portions of neither Reynolds, Takasugi nor Shreesha disclose this parallel storing and retrieving requirement of claim 60, (as discussed more fully above) this claim is not rendered obvious by their combination. Additionally, for the reasons discussed above, it was not proper to combine Shreesha with Reynolds or Takasugi, because there was no showing of a teaching, suggestion, or motivation to combine them. Withdrawal of the rejection to claim 60 is requested.

Claim 61 depends directly from claim 60, and includes all limitations of claim 60. Having established that claim 60 was not rendered obvious in view of the cited references, dependent claim 61 similarly is not obvious. Withdrawal of the rejections to claim 61 also is requested.

The Examiner rejected independent claims 62 and 64-67 under 35 U.S.C. §103(a) as being unpatentable over Reynolds in view of Takasugi, and further in view of Shreesha, and further in view of U.S. Patent No. 4,189,767 to Ahuja, and further in view of what the

Examiner considers Applicant-admitted prior art as applied to claim 1 above and further in view of U.S. Patent No. 6,018,354 to Jones and further in view of U.S. Patent No. 6,724,396 to Emmot. Certain other claims, which are dependent claims, were also rejected in view of these references. However those other claims have already been addressed above.

As a preliminary note, no less than six (6) prior art references have been combined to support the rejection of claims 62, 64-67. The need to combine so many references alone suggests that an obviousness rejection is not proper.

Claims 62, 64-67 are independent claims, and each has similar limitations that generally relate to the storing or retrieving pixel data (or data elements) in parallel to or from a first and second memory. For example, Claim 62 is representative and requires "retrieving pixel data for a first pixel and a second pixel in parallel from a first memory and a second memory, respectively, . . ." As discussed above in connection with claim 1, however, neither Reynolds, Takasugi nor Shreesha disclose this storing or retrieving pixel data in parallel to or from a first and second memory. As will be explained below, the remaining three references should not be used in connection with this limitation either.

One of the references, Jones, was not discussed in the office action in any detail in connection with its applicability to claims 62, 64-67. Therefore, there has been no *prima facie* showing by the Examiner in support of the obviousness rejection of these claims. A brief discussion of Jones appears on page 5 of the office action in connection with claim 5, but the Examiner made no reference of any relationship between claim 5 and claims 62, 64-67.

Assuming however that the Examiner intended to incorporate his discussion of Jones for claim 5 into the grounds for rejecting claims 62, 64-67, Jones would not support such a rejection. Jones relates to a method for accessing different banks of a DRAM. A two dimensional image is organized in a two dimensional grid pattern of cells, where each cell contains a matrix of pixels. The words associated with each cell occupy one page or less of a bank. Each cell is assigned a particular one of the two banks so that all data words associated with that particular cell are read from and written to one particular page of that particular bank. The cited portions of Jones (cited in connection with claim 5) however do not disclose this parallel storing and retrieving requirement of claims 62, 64-67.

Another of the references, Ahuja, also was not discussed in the office action in any level of detail in connection with its applicability to claims 62, 64-67, or in connection with any of the other claims. While Ahuja relates generally to the accessing of storage locations among a plurality of memory modules, there is no explanation in the office action of how this relates to image or pixel data, or the parallel storing/retrieving of such data. Moreover, there was no showing of a teaching, suggestion, or motivation to combine Ahuja with the other references. Therefore once again, there has been no *prima facie* showing in support of the obviousness rejection of these claims.

Emmot discloses a method for allocating texture data sets, among first and second areas of memory in a computer graphics system. Each texture map in a series of texture maps is divided into a set of blocks of data. Blocks of data from first map areas of odd level texture maps and from the second map areas of even level texture maps are stored in the first memory area. Blocks of data from the second map areas of odd level texture maps and from the first map areas of even level texture maps are stored in the second memory area. The blocks of data representing each texture map in the series of texture maps are stored in consecutive blocks of memory. The cited portions of Emmot, however, do not disclose the parallel storing and retrieving requirement of claims 62, 64-67. Therefore Emmot in combination with the other cited references do not render claims 62, 64-67 obvious.

Moreover, Applicant contends that it was not proper to combine Emmot with the other cited references. In order to combine references, the Examiner is required to show that there was a teaching, suggestion, or motivation to combine them. The reason given by the Examiner for combining Emmot is that it "reduces page miss penalty resulting in faster memory accesses." (Office Action, page 7). However as previously discussed, this is not a valid teaching, suggestion, or motivation. The recognition of a need does not render obvious the achievement that meets that need. Cardiac Pacemakers, Inc., v. St. Jude Medical, Inc., 381 F.3d 1371 (Fed. Cir. 2004).

In our case, the cited portions of Emmot generally deal with allocating texture data sets among first and second areas of memory in a computer graphics system to achieve faster memory accesses. However, the mere recognition of this need by Emmot does not render obvious Applicant's particular inventions in claims 62, 64-67 for achieving greater speed, *i.e.,* including the storing and retrieving of consecutive data elements or pixels (as the

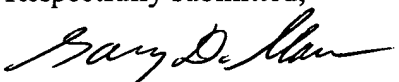
case may be) in parallel in two different orders. Thus for this additional reason, independent claims 62, 64-67 are not obvious over Reynolds in view of Takasugi, Shreesha, Ahuja, Jones and further in view of Emmot. Withdrawal of the rejections to claims 62, 64-67 is requested.

Claim 63 depends directly from claim 62, and includes all limitations of claim 62. Having established that claim 62 was not rendered obvious in view of the cited references, dependent claim 63 similarly is not obvious. Withdrawal of the rejection to claim 63 also is requested.

CONCLUSION

For all the reasons advanced above, Applicant submits that the application is in a condition for allowance, and that action is earnestly solicited.

Respectfully submitted,



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Attachments: Six sheets of replacement drawings

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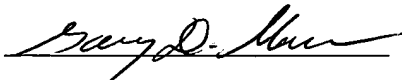 6/10/2005

Gary D. Mann (Date)